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□ Examination time: 120 min. □ Write your name and student number in the space provided above. □ This examination is closed book. □ There are 3 questions. The points for each question are given in the square brackets, next to the question title. The overall maximum score is 100. This final exam weighs 40% of your final grade.

CS303 DIGITAL DESIGN FINAL EXAM

Digital Logic Session 44; Page 1/5 Spring 2003 COE/EE 243 Sample Final Exam From Fall 98 Solutions Show your work. Do NOT use a calculator! 1. (9 pts) Complete the following table of

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equivalent values. Binary Octal Decimal Hexadecimal 1011.0011 13.14 11.1875 B.3 11101.11111101
35.77 29.99 1D.FD 11011.010011 33.23 27 19 64 1B.4C 2. (12 pts ...

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machine, asynchronous sequential logic, binary systems, Boolean algebra and logic gates, combinational logics, digital integrated circuits, DLD experiments, MSI and PLD components, registers counters ...

Digital Logic Design MCQs: Multiple Choice Questions and ...

ENEL 353 - Digital Circuits Final Examination. Name: Lecture Section: ID#: ENEL 353 - Digital Circuits Final Examination. Wednesday, December 17, 2008 Time: 8:00 - 11:00 AM Auxiliary Gymnasium. L01 - Norm Bartley L02 - Svetlana Yanushkevich Instructions: Time allowed is 3 hours. Please review the examination rules on Page 2.

ENEL 353 - Digital Circuits Final Examination

Evaluation Strategy : Your final grade in this course will be based on seven quizzes (50% total), one mid-term exam (20%) and a comprehensive final exam (30%). We'll drop 2 quizzes with the lowest score. No alternative test arrangements can be made. Graded quizzes and exams will be returned through the distribution center.

CS 151 SQ08 Digital Logic Design

pass the exam. requires at least . 11 points. from A1 + A2 , if fewer points we will not look at the rest of your exam. Part B (Design problems) contains two design problems of a total of 10 points. Part B is . corrected only if there are at . least 11p. from the exam A- Part. NOTE !

Written exam with solutions IE1204-5 Digital Design Friday ...

ECE-2 78 : Digital Logic Design Fall 2016. Solutions - Midterm Exam (October 13 th @ 5:30 pm)

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Presentation and clarity are very important! Show your procedure! **PROBLEM 1 (20 PTS)** a) Complete the following table. The decimal numbers are unsigned: (6 pts.) Decimal BCD Binary Reflective Gray Code
52 01010010 110100 101110. 34 00110100 100010 110011

Exam January Fall 2016. questions and answers - ECE 278 ...

Final Examination EE 203-Digital Systems DESIGN(Fall2015) MEFUniversity Assigned: 12:00am on January 4, 2016. Due: 1:50pm on January 4, 2016. Location: A201, MEF University Instructor: S,uyab S,. Arslan. Name: Student ID: Instructions 1. For every design you make or the solution you present, please show every step you take. I am looking

Final Examination - suayb arslan

Numbers. systems, and codes. Boolean algebra and logic minimization methods. Combinational and sequential design and using logic gates and flip flops. Memory and programmable logic, register transfer and computer operations, control logic design. Computer instructions and addressing modes, and design of a CPU input-output communication memory management Practice Exams Digital Design_Spring ...

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